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09046671

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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EXAMINER

ART UNIT	PAPER NUMBER
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DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.

09/046,671

Applicant(s)

TAKITA ET AL.

Examiner

Kurt M. Eaton

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

- 1) ☒ Responsive to communication(s) filed on 26 June 2000.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) 8-22 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
- a) ☐ All b) ☐ Some * c) ☐ None of the CERTIFIED copies of the priority documents have been:
1. ☐ received
2. ☐ received in Application No. (Series Code / Serial Number) _____
3. ☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

- 15) ☐ Notice of References Cited (PTO-892)
- 16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 18) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 19) ☐ Notice of Informal Patent Application (PTO-152)
- 20) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Subject matter that the specification as originally filed fails to adequately describe is included in newly amended claim 1, more specifically, "wherein a concentration of an impurity of the semiconductor region of the first conduction type is almost equal to a concentration of an impurity of the semiconductor substrate". How equal is "almost" equal? Does it mean "substantially" equal, as if it were intended that the two regions were equal in impurity concentration? Does "almost" mean that the two regions intentionally have different impurity concentrations? Why do the two regions have impurity concentrations which are "almost equal"? How are the two regions formed to have "almost equal" impurity concentrations?

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 5-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

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Regarding claims 5-7, the phrase "and/or" renders the claim indefinite because it is unclear whether both the first and second semiconductor elements are memory cells or whether just one of the first and second semiconductor elements is a memory cell. The subject matter found within the claims must be written in a positive sense and the present alternative sense needs to be removed in order to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuda et al..

In re claim 1, Kikuda et al. (herein referred to as Kikuda) shows, in an analogous art related to a semiconductor device, in Figure 20 a semiconductor substrate (206) of a first conduction type, labeled "p substrate"; a buried semiconductor layer (bottom portion of item (220) found laterally under item (222)) of a second conduction type forming in a first region of the semiconductor substrate, spaced from a surface of the semiconductor substrate; a semiconductor region of the second conduction type (upper portion of item (220) that is not part of the buried semiconductor layer) extending from the surface of the semiconductor substrate to a peripheral portion of the buried semiconductor layer and; a semiconductor region (222) of the first conduction type, labeled

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"p well", formed in the semiconductor substrate surrounded by the buried semiconductor layer and the semiconductor region of the second conduction type {column 15, lines 25-34}.

Kikuda does not show wherein a concentration of an impurity of the semiconductor region of the first conduction type is almost equal to a concentration on an impurity of the semiconductor substrate.

It would have been obvious to one of ordinary skill in the art at the time the invention was made that since the semiconductor substrate and the semiconductor region of the first conduction type were both labeled as "p substrate" and "p well", respectively, it would be reasonable for one of ordinary skill in the art to deduce that the semiconductor substrate and the semiconductor region of the first conduction type had almost equal concentrations of impurities of the first conduction type.

In re claim 2, Kikuda further shows in Figure 20 a first semiconductor element (232) formed in the first conduction type region; and a second semiconductor element (226) formed in a second region different from the first region of the semiconductor substrate, wherein the first conduction type semiconductor region is connected to a first potential (V_{BB}) and wherein the second region of the semiconductor substrate is connected to a second potential (V_{SS}) different from the first potential.

In re claim 3, Kikuda shows in Figure 20 wherein the second conduction type semiconductor region is extended over a third region adjacent to the first region of the semiconductor substrate; wherein the semiconductor device further includes a third semiconductor element (228) formed in the third region of the second conduction type semiconductor region; and wherein the second conduction type semiconductor region is connected to a third potential (V_{CC}) different at least the first potential or the second potential.

In re claim 4, Kikuda substantially discloses the invention as claimed but fails to show a well of the first conduction type formed in a fourth region in the third region; and a fourth semiconductor element formed in the first conduction type well, wherein the first conduction type well is connected to a fourth potential different from at least the first potential.

It would have been obvious to one of ordinary skill in the art at the time the invention was made for the semiconductor device to have a well of the first conduction type formed in a fourth region in the third region and a fourth semiconductor element formed in the first conduction type well, wherein the first conduction type well is connected to a fourth potential different from at least the first potential since this would require duplication of structural parts from within the first region (i.e., duplication of the semiconductor region of the first conduction type formed in the semiconductor substrate surrounded by the buried semiconductor layer and the semiconductor region of the second conduction type which extends from the surface of the semiconductor substrate to a peripheral portion of the buried semiconductor layer; duplication of the first semiconductor element formed in the first conduction type region; and duplication of the first conduction type semiconductor region being connected to the first potential) to within the third region adjacent to the first region of the semiconductor substrate and mere duplication of essential structures of a device involves only routine skill in the art. Furthermore, the specification contains no disclosure of either the critical nature of the claimed duplicated structure or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen addition of duplicated structures or upon another variable recited in a claim, the applicant must show that the particular added structures are critical.

In re claims 5-7, Kikuda shows in Figure 20 wherein the first semiconductor element and/or the second semiconductor element is a memory cell.

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Response to Arguments

7. Applicant's arguments with respect to claims 1-7 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Paper related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2823 Fax Center number is (703) 308-7722 or -7724. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

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Any inquiry concerning this communication of earlier communication from the examiner should be directed to **Kurt Eaton** at **(703) 305-0383** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via kurt.eaton@uspto.gov.



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